FILE 'USPAT' ENTERED AT 13:39:02 ON 08 APR 1999

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                 W E L C O M E   T O   T H E             *
*            U. S.  P A T E N T   T E X T   F I L E       *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
```

=> s (transaction# or task# or job#) (p) arbit?

```
        31217 TRANSACTION#
        95422 TASK#
        35905 JOB#
       106094 ARBIT?
L1       2729 (TRANSACTION# OR TASK# OR JOB#) (P) ARBIT?
```

=> s l1 (p) (order or later)

```
      1427137 ORDER
       376971 LATER
L2        613 L1 (P) (ORDER OR LATER)
```

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* * * * * * RECONNECTED TO U.S. Patent & Trademark Office * * * * * *
SESSION RESUMED IN FILE 'USPAT' AT 14:16:24 ON 08 APR 1999
FILE 'USPAT' ENTERED AT 14:16:24 ON 08 APR 1999
=> d his


     (FILE 'USPAT' ENTERED AT 14:12:06 ON 08 APR 1999)
L1        1558 S (TRANSACTION# OR TASK#) (10A) ((OUT OF ORDER) OR LATER)
L2          39 S L1 (P) ARBIT?
```

s 5006982/pn or 5822772/pn or 5682512/pn

```
              1 5006982/PN
              1 5822772/PN
              1 5682512/PN
L1            3 5006982/PN OR 5822772/PN OR 5682512/PN
```

=> d 1-3

1. **5,822,772**, Oct. 13, 1998, Memory controller and method of memory access sequence recordering that eliminates page miss and row miss penalties; Cheng-Sheng Chan, et al., 711/158; 710/52, 57; 711/5, 105, 150, 151 [IMAGE AVAILABLE]

2. **5,682,512**, Oct. 28, 1997, Use of deferred bus access for address translation in a shared memory clustered computer system; R. Scott Tetrick, 711/202; 345/974; 710/128 [IMAGE AVAILABLE]

3. **5,006,982**, Apr. 9, 1991, Method of increasing the bandwidth of a packet bus by reordering reply packets; Ronald J. Ebersole, et al., 710/263; 364/229.2, 230.1, 242.8, 242.92, 284.1, 284.3, DIG.1 [IMAGE AVAILABLE]